Silicon Technology Leadership and the New Scaling Paradigm

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Logic Technology Development
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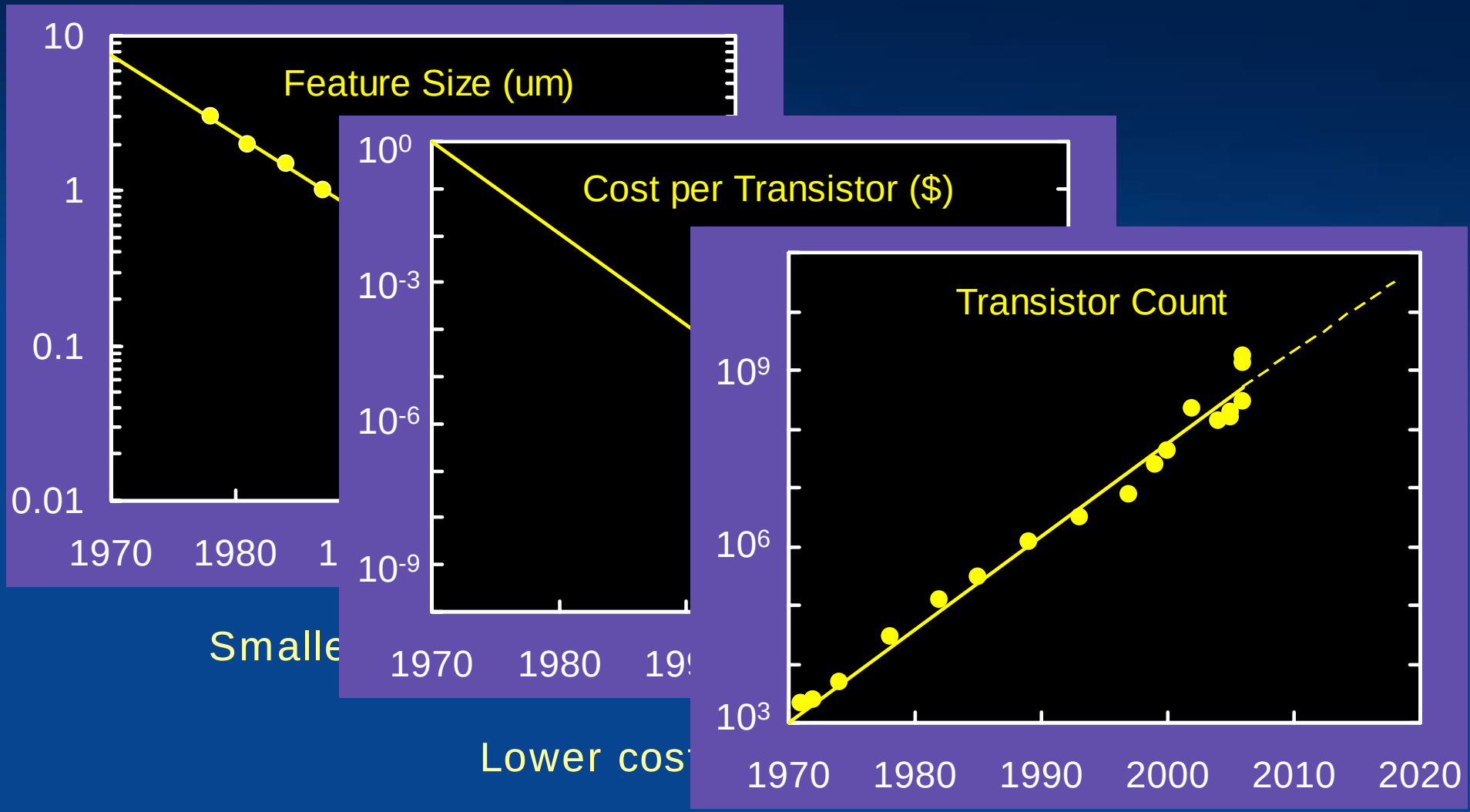
Key Messages

- Intel's R&D pipeline will sustain Moore's Law for the foreseeable future
- Intel technologies are proliferated into a world-wide network of factories and Intel has a large presence in China
- 45 nm high-k + metal gate is the most significant innovation in transistor technology in 40 years
- Intel continues its unwavering commitment to support R&D for future technologies and to deliver the benefits of Moore's Law to our customers

Outline

- Intel's Silicon R&D Pipeline
- Technologies in Manufacturing
- 45 nm High-k + Metal Gate Transistors
- Future Technology Options
- Summary

Delivering Moore's Law



Enables more transistors and increased performance

Intel's Silicon R&D Pipeline

Research		Development	Manufacturing
Identify Ideas/Options		Select Features Make it Work	High Volume Manufacturing
External	Internal		
Consortia	Oregon	Oregon	Oregon
Universities	California		California
Investment	Arizona		Arizona
Suppliers			New Mexico
Nat'l Labs			Massachusetts
			Israel
			Ireland

Intel's Silicon R&D Pipeline

Research	Development	Manufacturing
Identify Ideas/Options	Select Features Make it Work	High Volume Manufacturing
External: Consortia, Universities, Investment, Suppliers, Nat'l Labs Internal: Oregon, California, Arizona	Oregon ⇕ Product Design	Oregon, California, Arizona, New Mexico, Massachusetts, Israel, Ireland

Close collaboration between process development and product design

intel

Intel's Silicon R&D Pipeline

Research Development Manufacturing

Continuous flow of new technologies from research to development to manufacturing

Wafer Fab and Assembly / Test Sites

Intel Presence in China

University Collaboration

Over 40 universities, including...

Beijing University

Qinghau University

Fudan University

Shanghai Jiaotong University

Univ. of Electronics Science and Technology of China

Intel Presence in China

Research & Development

Beijing: Computing and communication architecture

Shanghai: Software and emerging market PC platforms

Shanghai: Package technology and flash design

Intel Presence in China

Assembly/Test

Shanghai

Chengdu

Wafer Fab

Dalian (2010)

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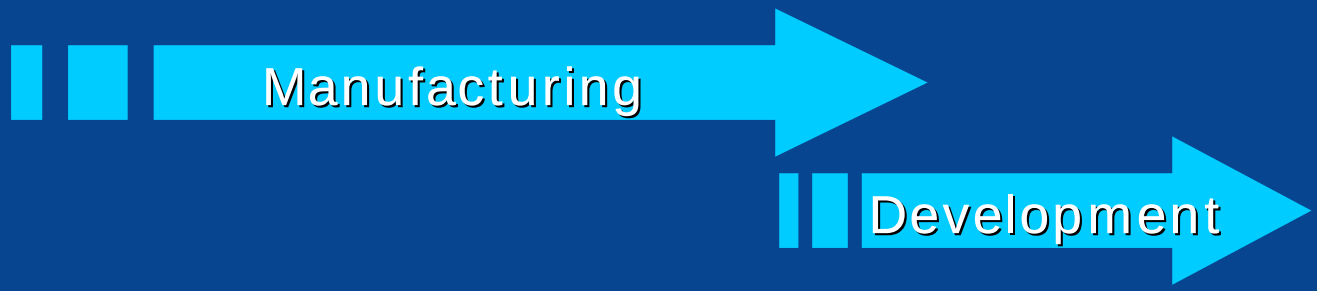
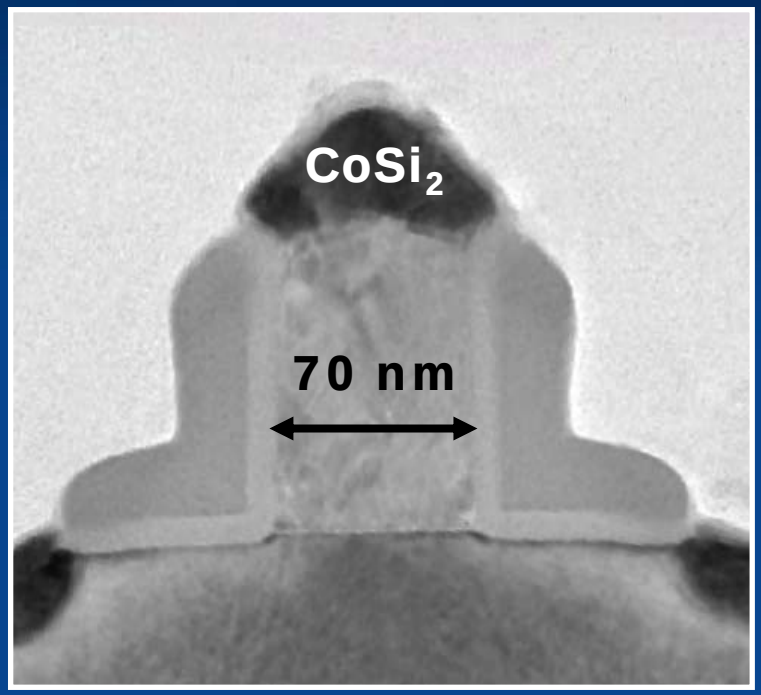
Logic Technology Evolution

Process Name	P860	P1262	P1264	P1266	P1268
Lithography	130 nm	90 nm	65 nm	45 nm	32 nm
1st Production	2001	2003	2005	2007	2009
Wafer (mm)	200/300	300	300	300	300



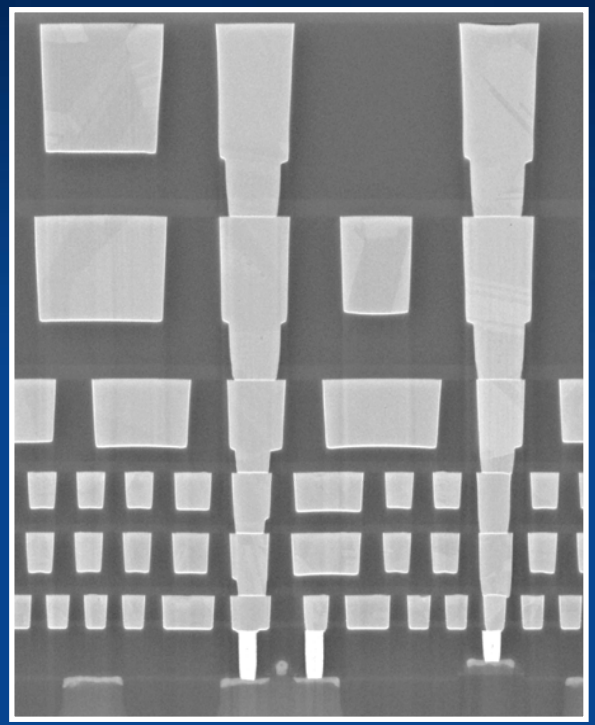
130 nm Technology - 2001

Transistors



1.5 nm gate oxide

Interconnects

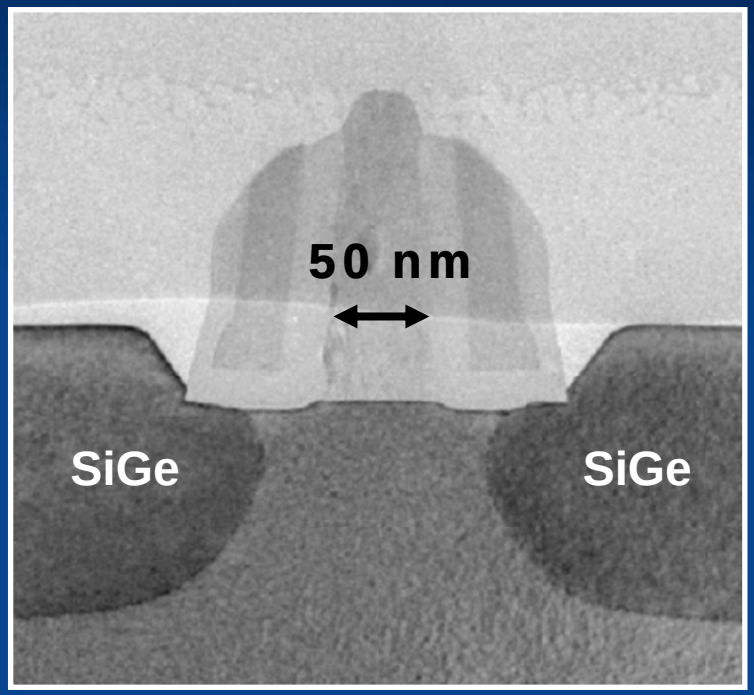


6 copper layers

SiOF dielectric

90 nm Technology - 2003

Transistors

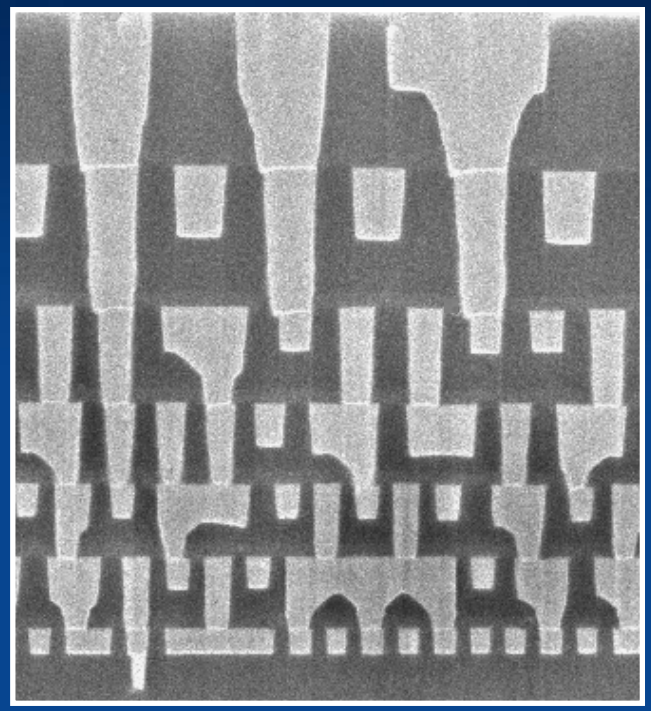


1.2 nm gate oxide

NiSi for low resistance

SiGe strained silicon technology

Interconnects

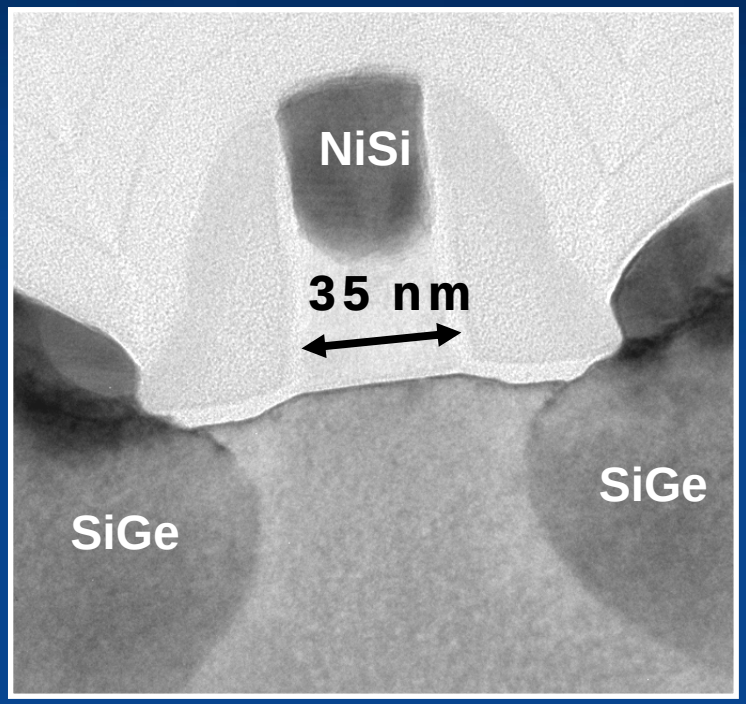


7 copper layers

Low-k carbon-doped oxide

65 nm Technology - 2005

Transistors

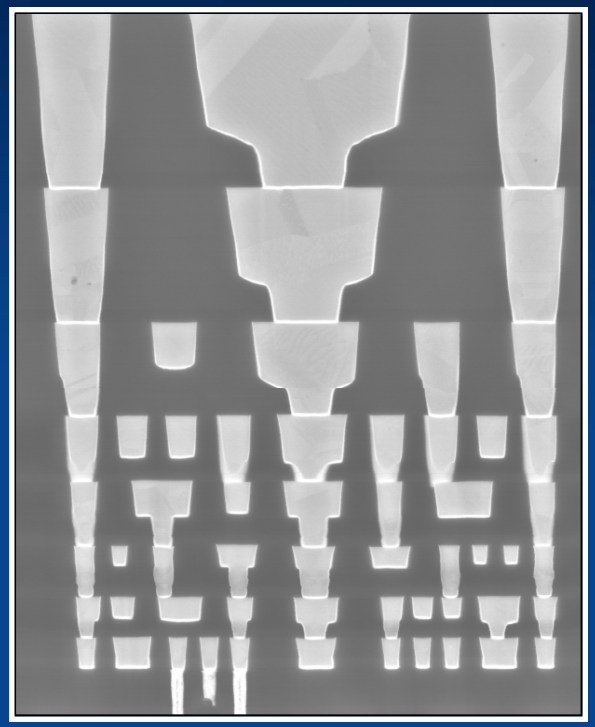


1.2 nm gate oxide

2ND gen. SiGe strained silicon

Industry-leading performance

Interconnects



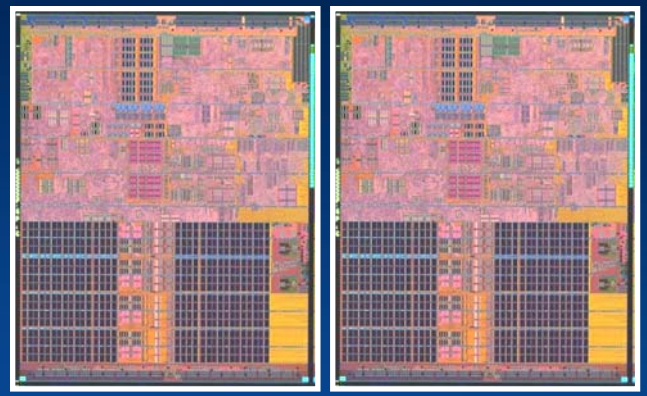
8 copper layers

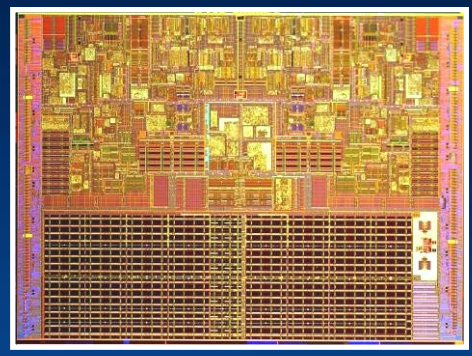
Low-k carbon-doped oxide

SiCN etch-stop layer

65 nm Dual Core Microprocessors

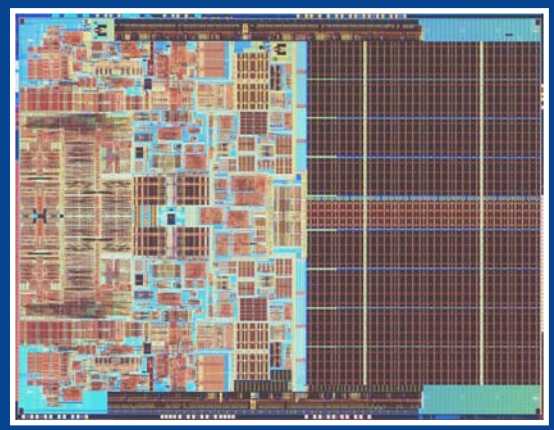
Intel Pentium® D Processor

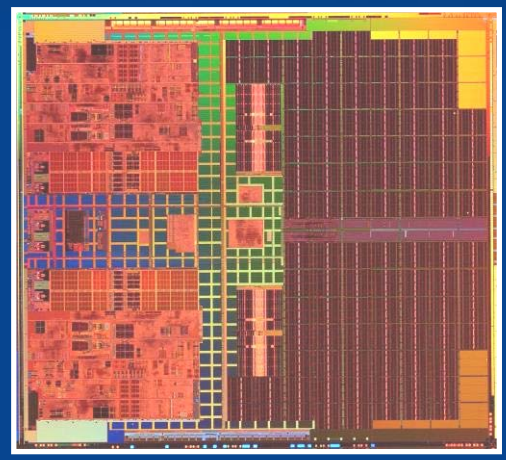




Intel Core™ Duo Processor

Intel Core™2 Duo Processor





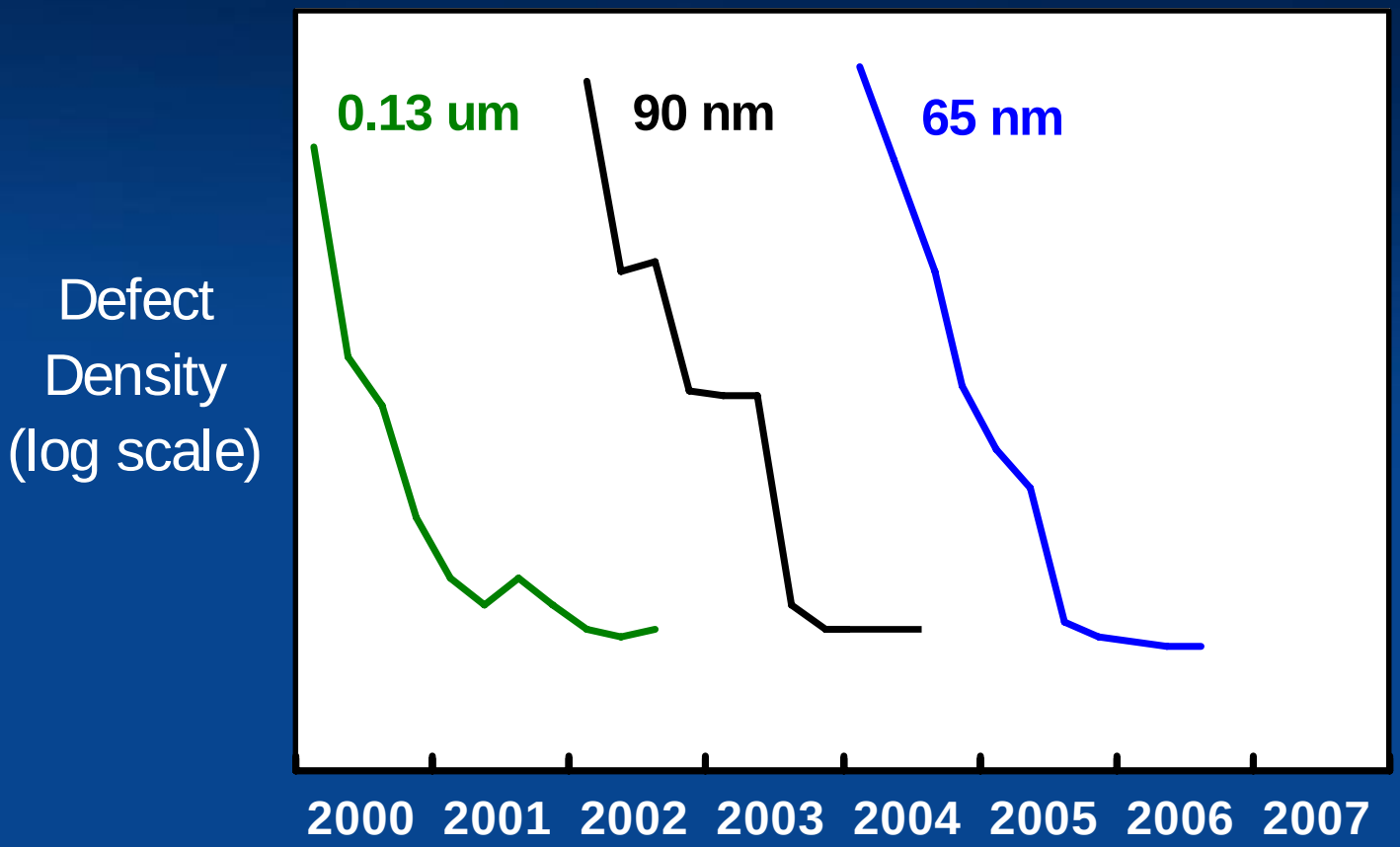
Intel Dual-Core Xeon® 7100 Processor

Intel has many 65 nm products

Volume production started in October 2005

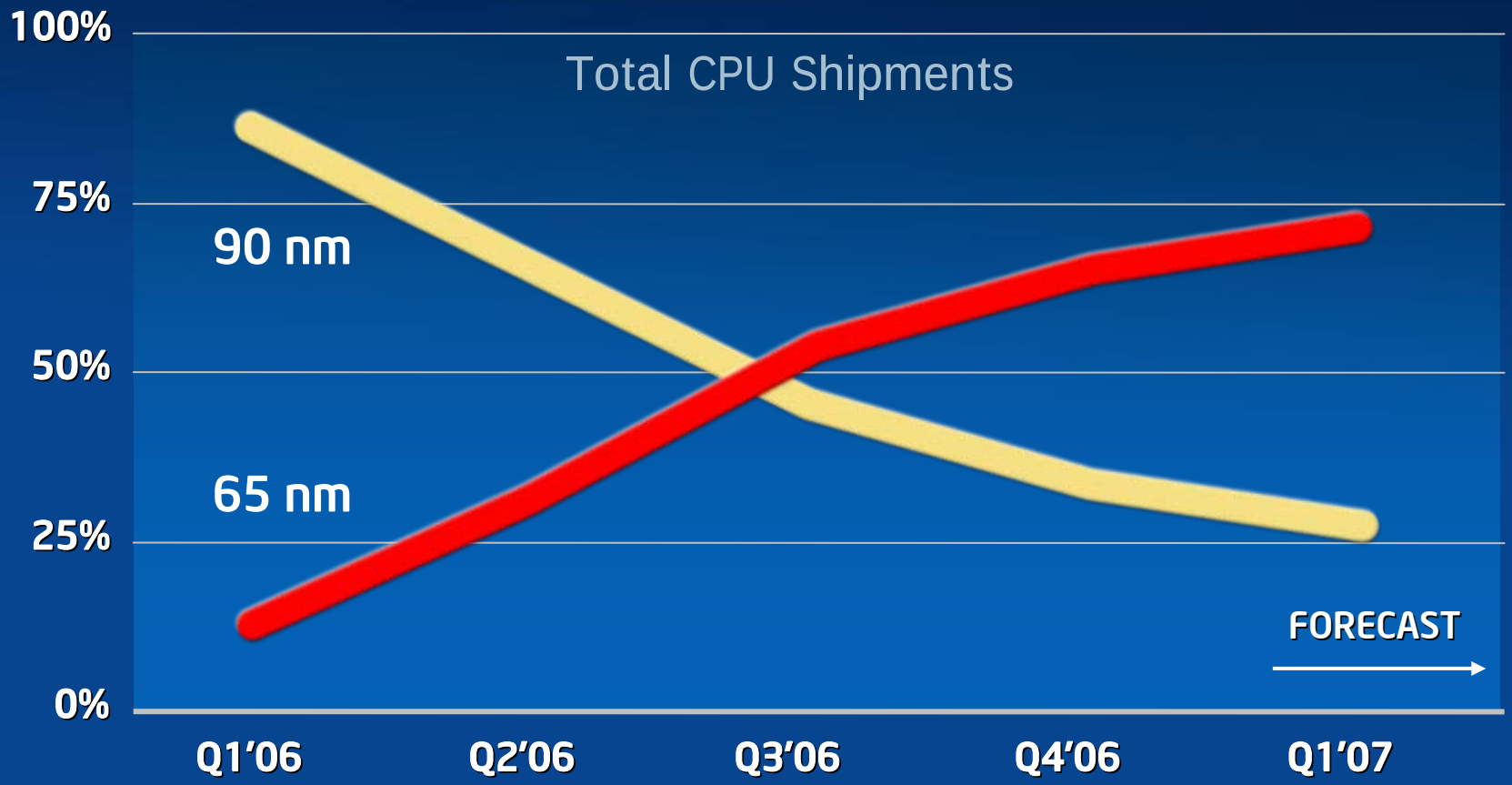
intel

65 nm Yield Improvement Trend



65 nm is Intel's highest yielding process ever

Intel Only:
Process + Products + Production



65 nm crossover occurred in Q3 '06

>70 million units shipped in 2006

65 nm Summary

- Intel has been shipping 65 nm processors since October 2005, more than one year ahead of the competition
- Intel shipped >70 million 65 nm processors by the end of 2006
- Only Intel has three 65 nm / 300 mm fabs shipping in volume

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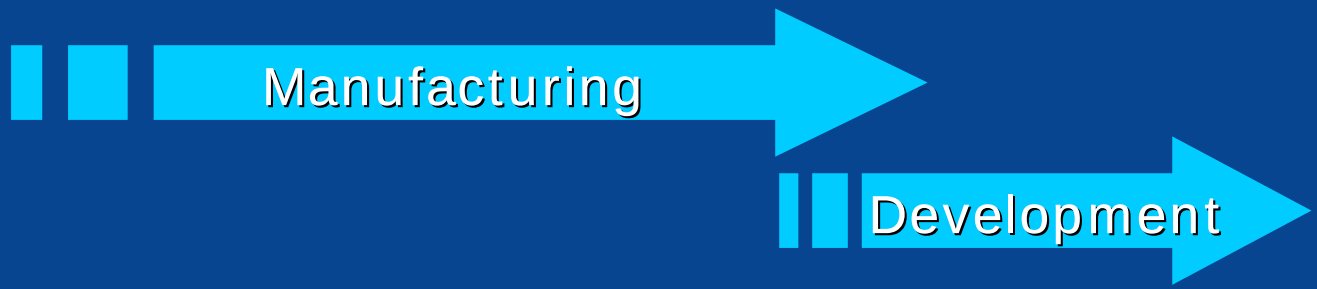


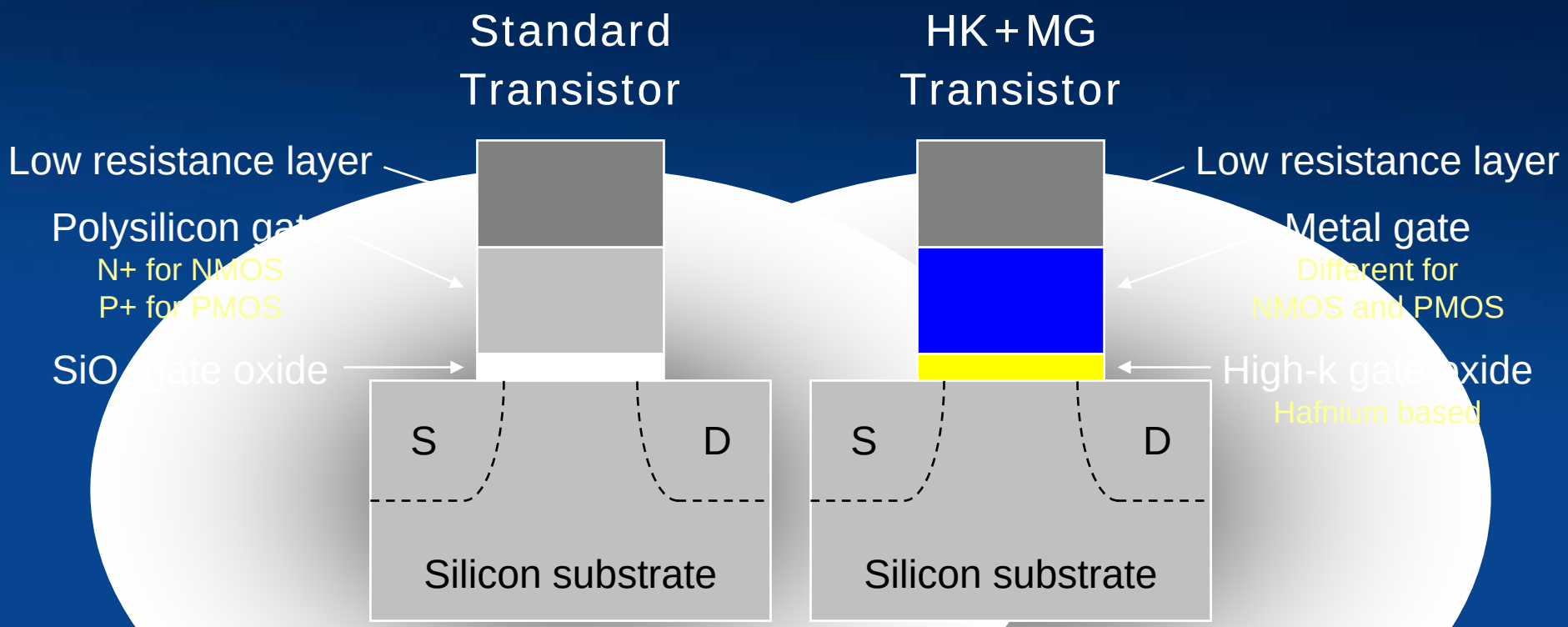
45 nm Technology Benefits

45 nm benefits compared to 65 nm

~2x	improvement in transistor density, for either smaller chip size or increased transistor count
~30%	reduction in transistor switching power
>20%	improvement in transistor switching speed or
>5x	reduction in source-drain leakage power
>10x	reduction in gate oxide leakage power

These performance and leakage improvements would not be possible without high-k + metal gate

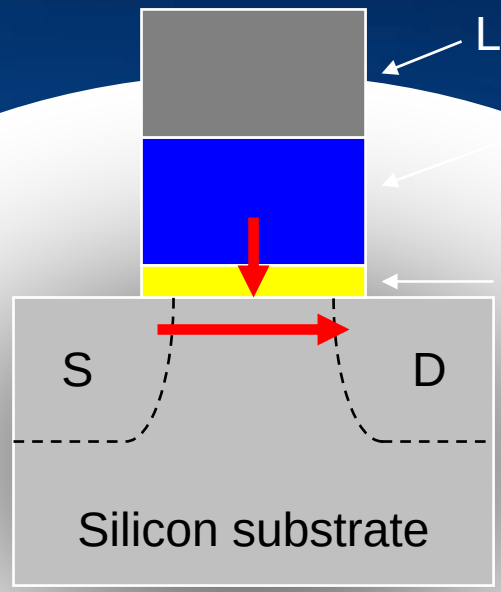
High-k + Metal Gate Transistors



High-k + metal gate transistors provide significant performance increase and leakage reduction, ensuring continuation of Moore's Law

High-k + Metal Gate Transistors

HK+MG
Transistor



Metal Gate

Increases the gate field effect

High-k Dielectric

Increases the gate field effect

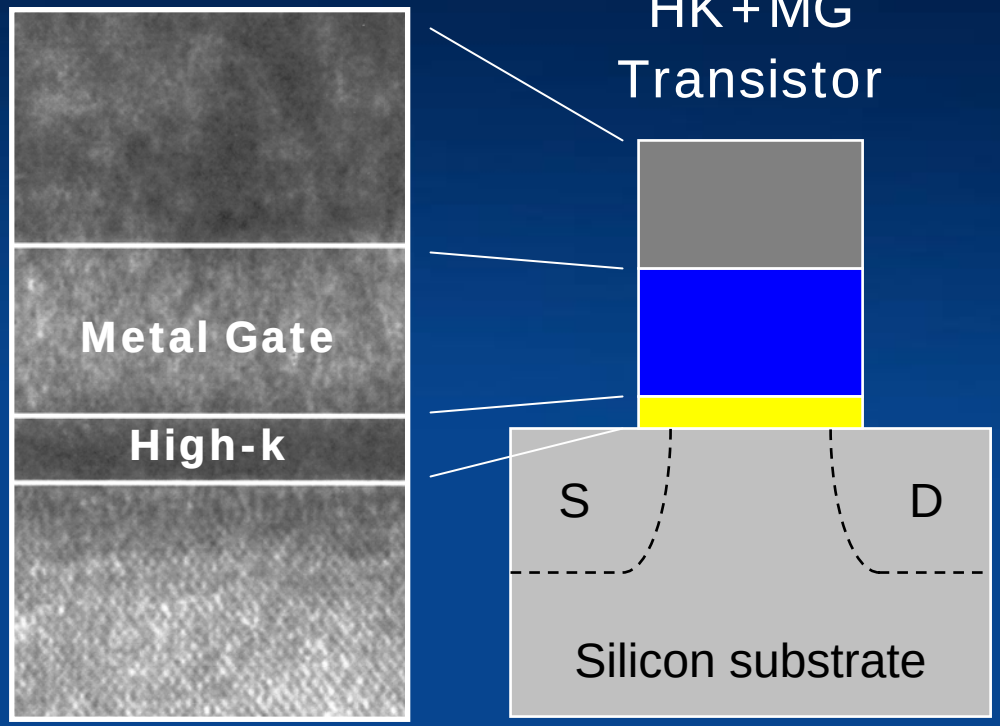
Allows use of thicker dielectric
to reduce gate leakage

High-k + Metal Gate Combined

Transistor drive current increased >20%
Or source-drain leakage reduced >5x
Gate oxide leakage reduced >10x

High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume

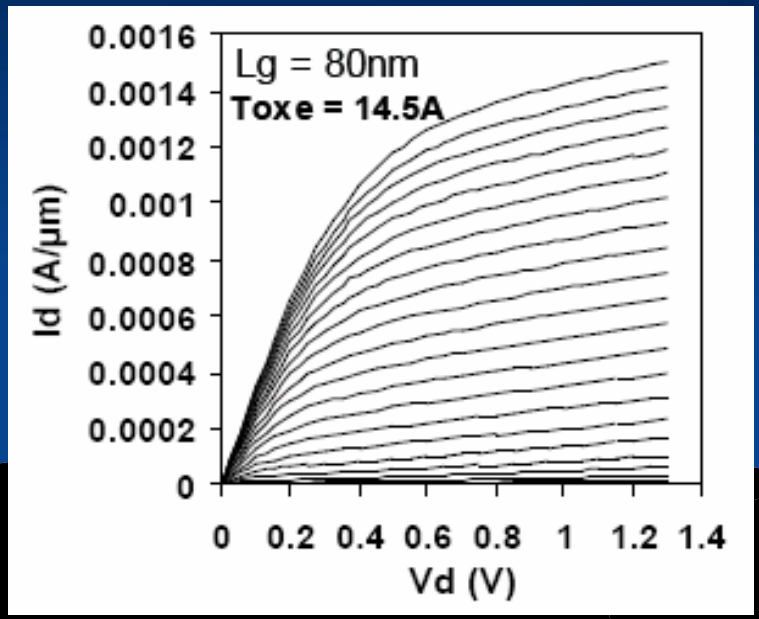


"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"

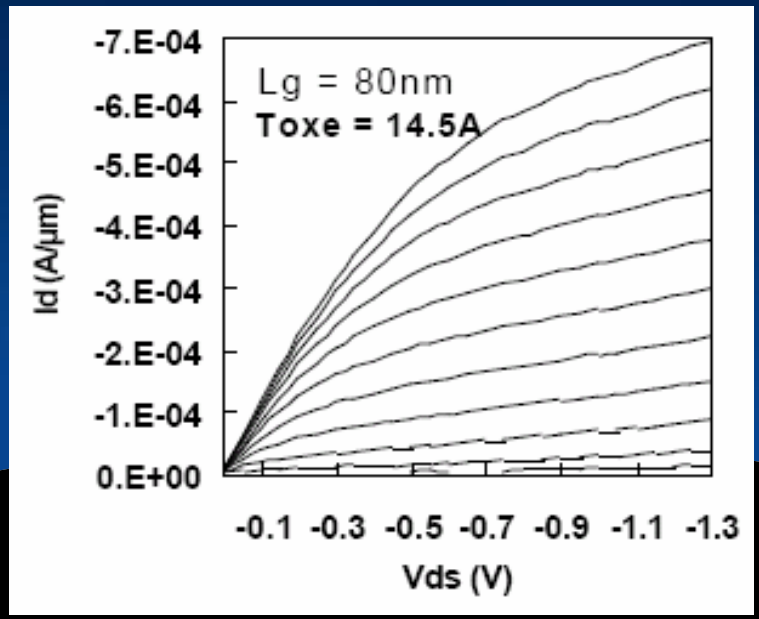
— Gordon Moore

2003 High-k + Metal Gate Transistors

NMOS



PMOS



R. Chau, International Workshop on Gate Insulator, Tokyo, Japan, Nov. 2003

Intel's Components Research group announced first working high-k + metal gate transistors in 2003

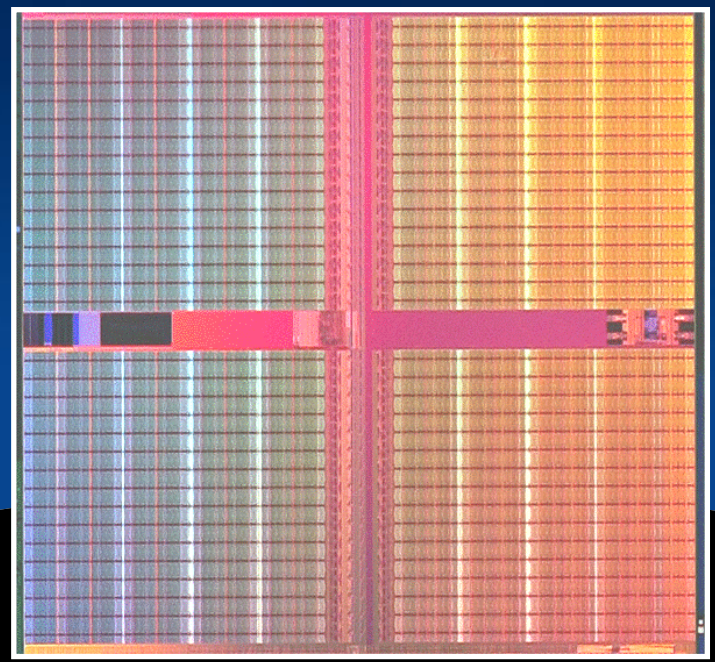
45 nm SRAM Test Chip

0.346 um^2 cell

153 Mbit density

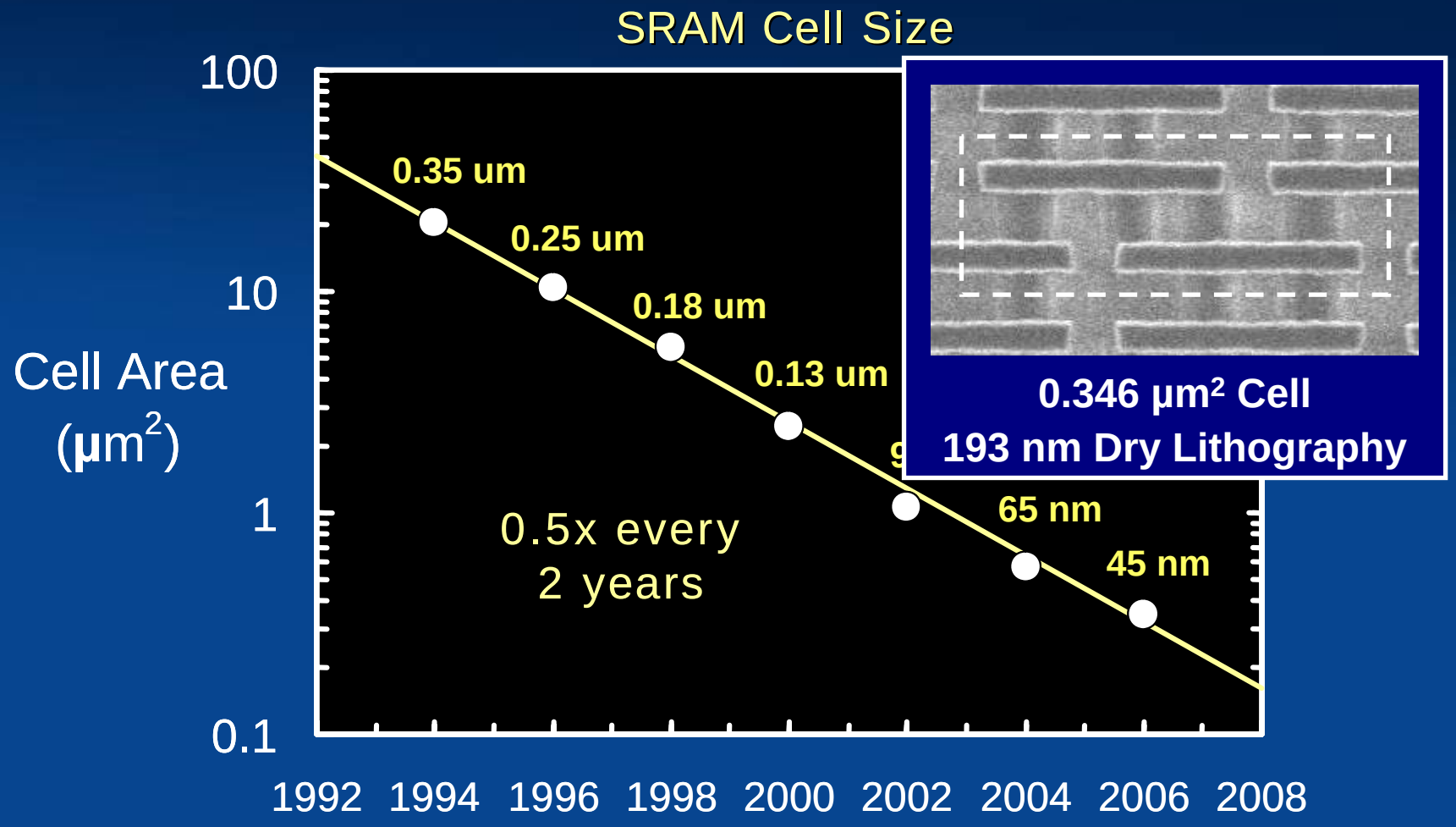
>1 billion transistors

Fully functional in Jan. ‘06



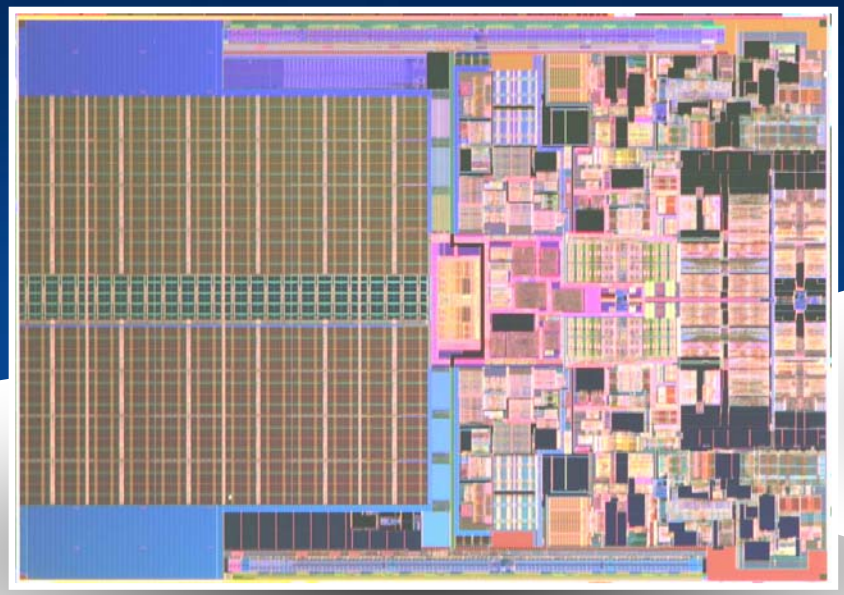
SRAM incorporated all process features used on 45 nm microprocessors, including high-k + metal gate

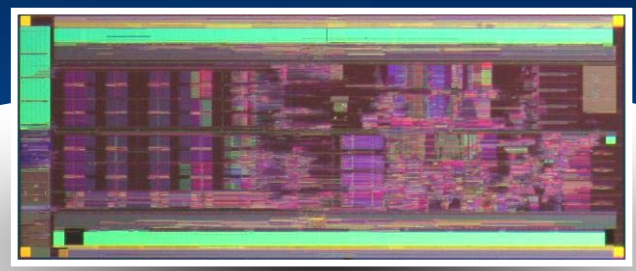
Density Scaling on Track



Cost-effective 193 nm dry lithography extended to 45 nm generation

World's First Working 45 nm CPUs





Penryn

45 nm Hi-k Intel® Core™2 and Intel Xeon™ processors

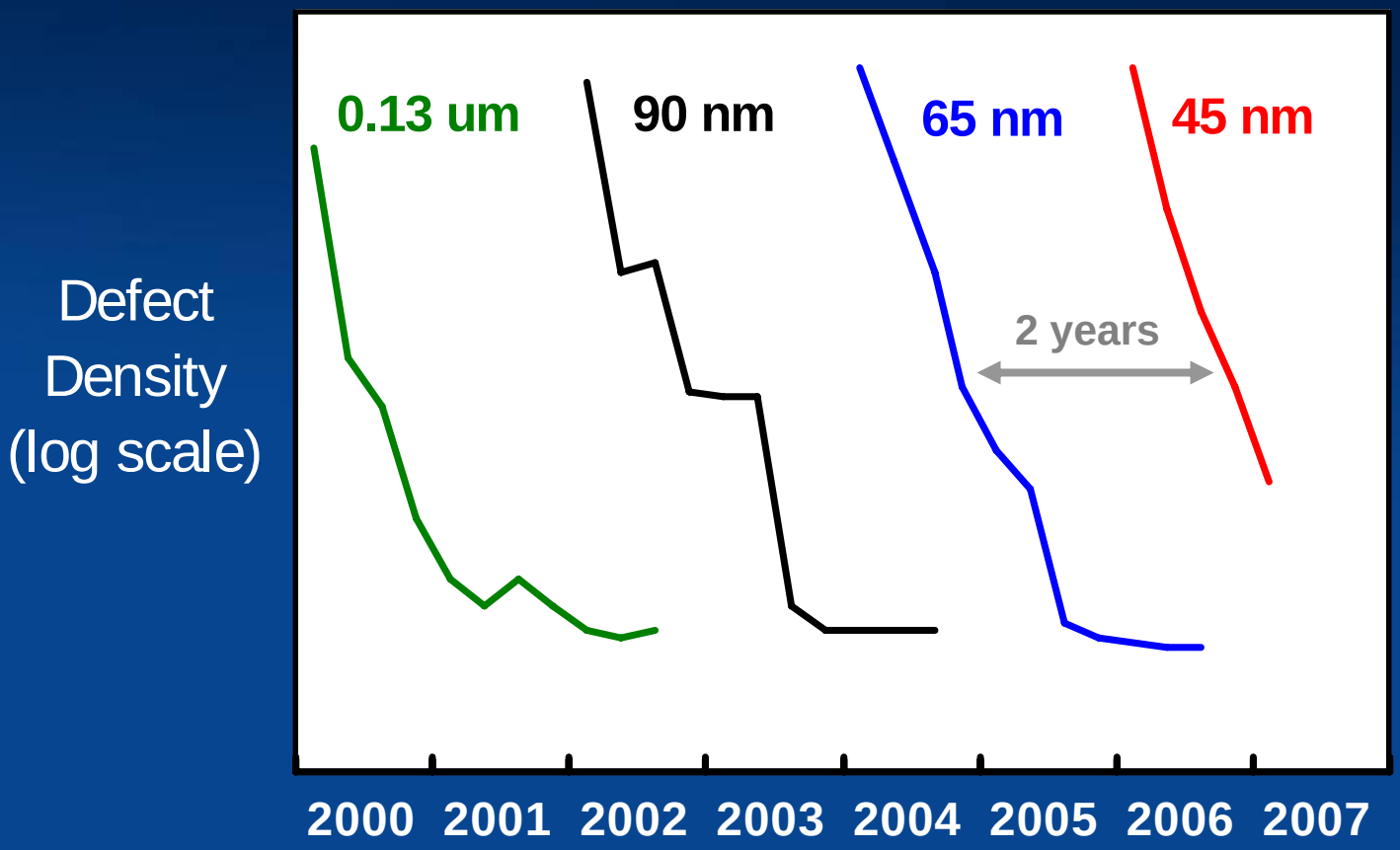
Mobile, Desktop, Workstation, and Server Optimized

Silverthorne

45 nm Hi-k new low power microarchitecture

Mobile Internet Devices and Ultra-Mobile PCs

45 nm Yield Improvement Trend



45 nm defect reduction trend at expected 2 year offset

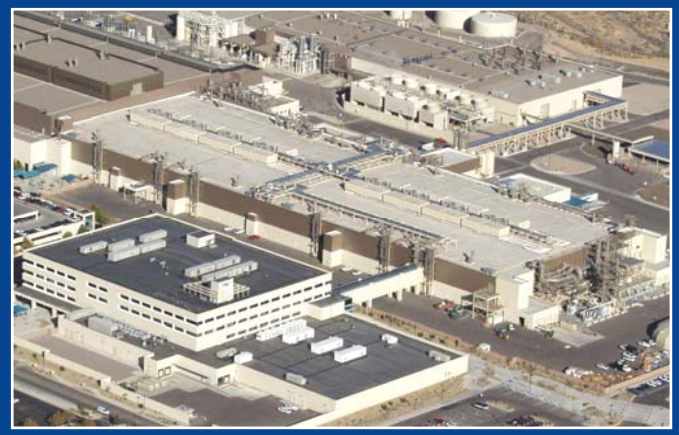
45 nm on track for production in 2H ‘07

45 nm Manufacturing Fabs

D1D Oregon - 2H ‘07

Fab 32 Arizona - 2H ‘07

Fab 28 Israel - 1H ‘08



Fab 11X New Mexico - 2H ‘08

45 nm Summary

- Intel has achieved a significant breakthrough in transistor technology by developing 45 nm high-k + metal gate transistors
- Working 45 nm microprocessors have been made using these revolutionary high-k + metal gate transistors
- Intel's 45 nm products are on track to begin production in 2H '07
- Intel is pulling further ahead of the competition

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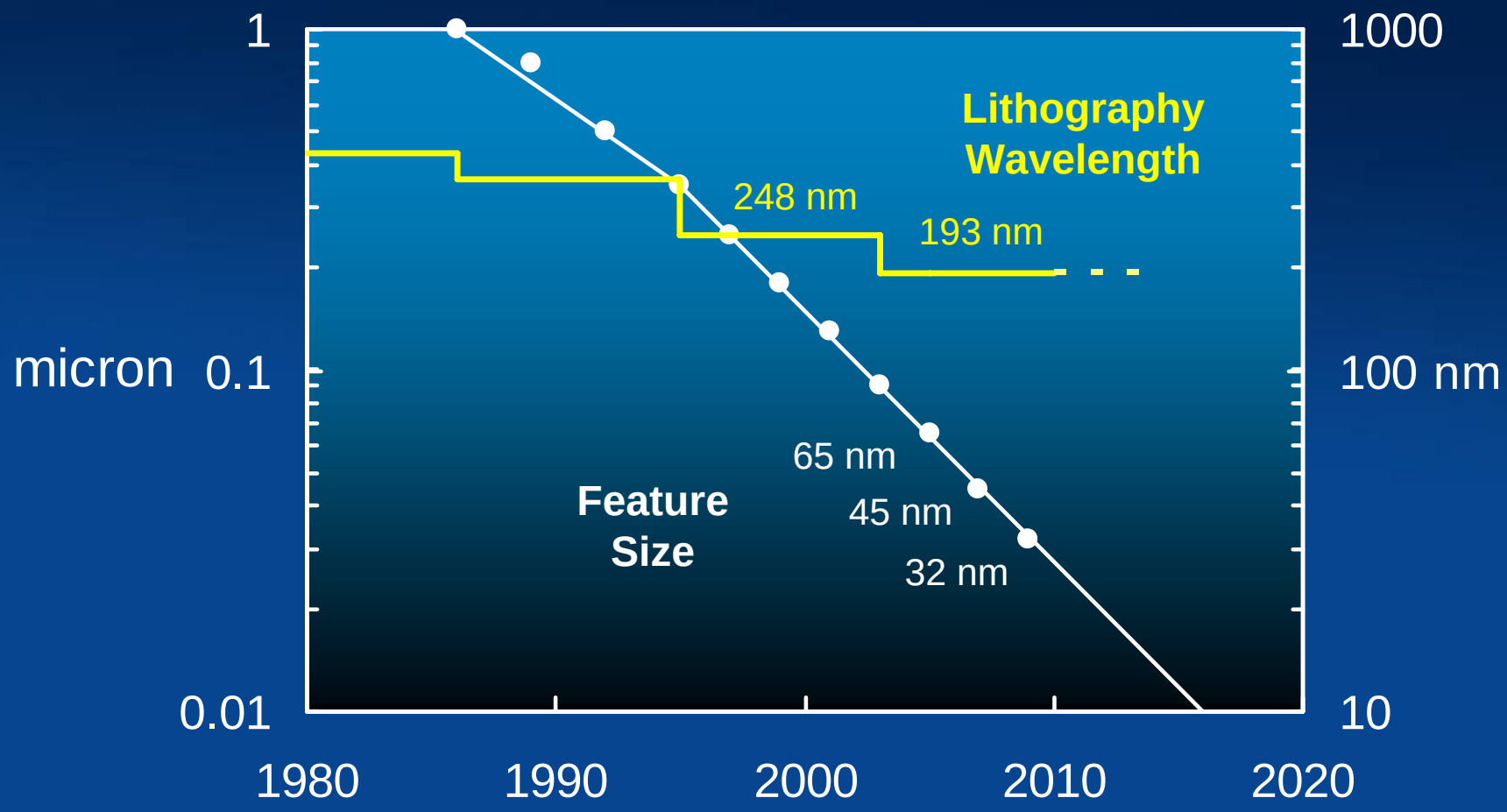
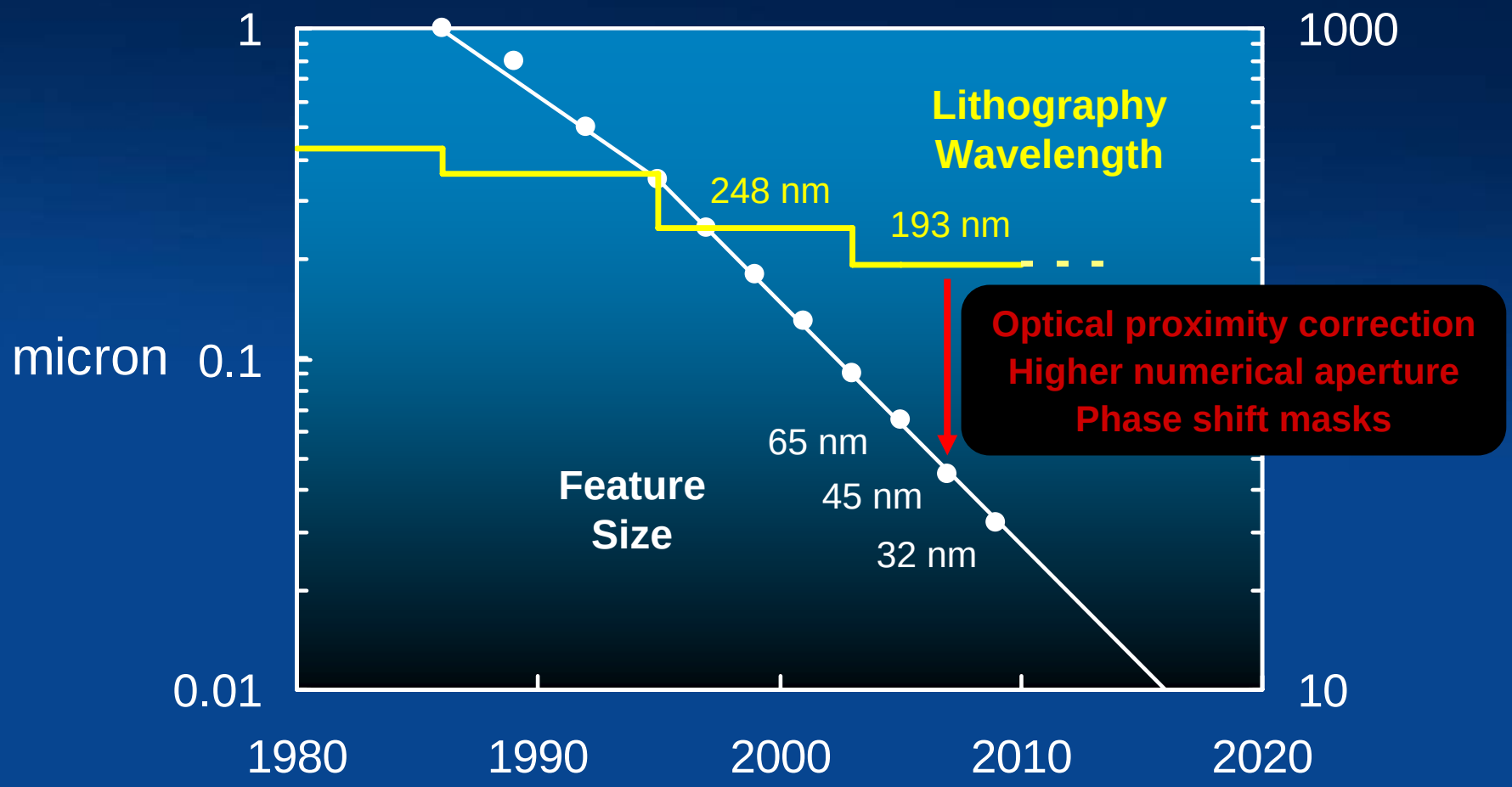
Lithography



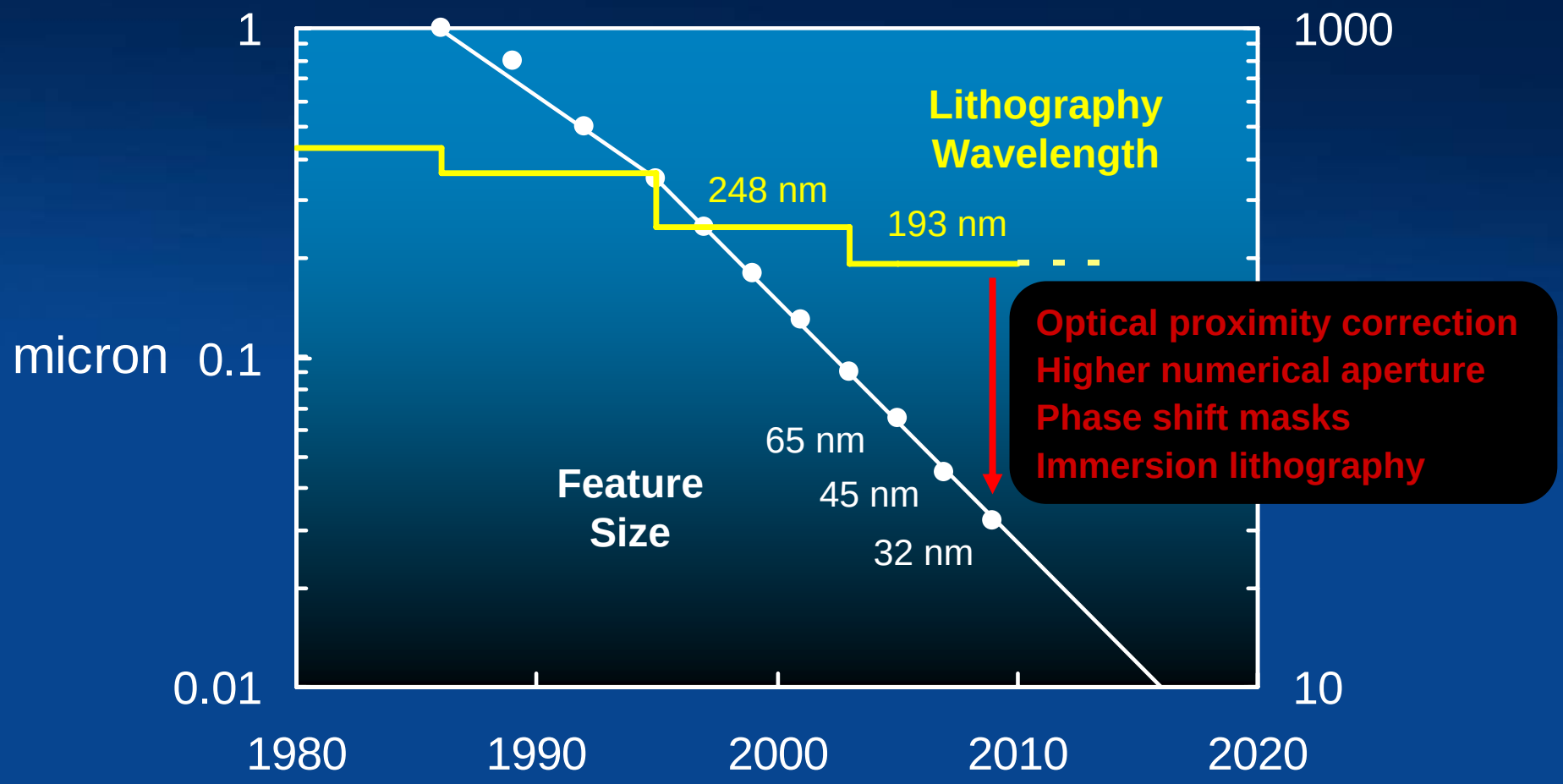
Minimum feature size is scaling faster than wavelength

Lithography



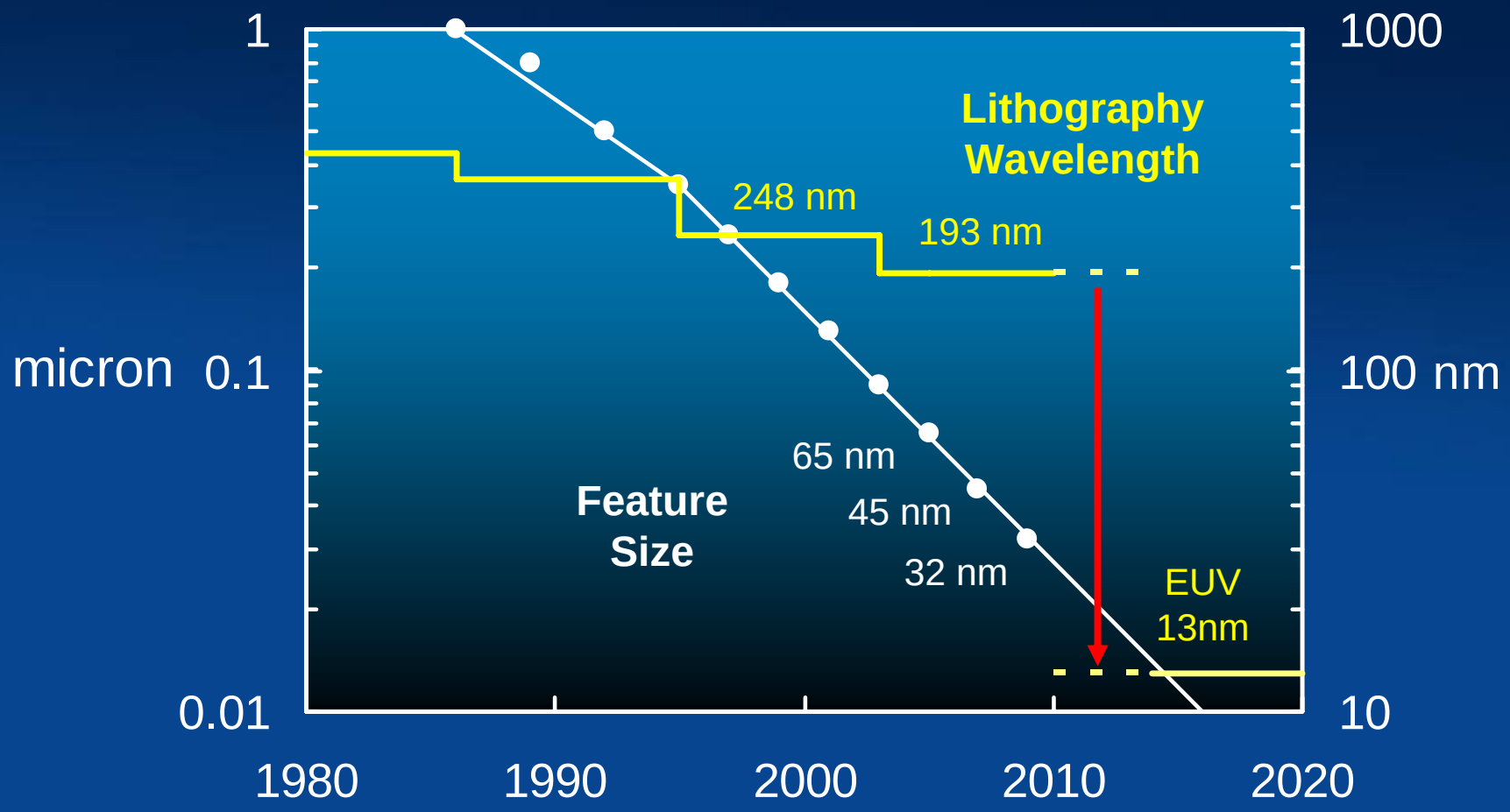
Enhancements have extended 193 nm dry lithography to the 45 nm generation

Lithography



Immersion lithography will extend 193 nm at least to the 32 nm generation

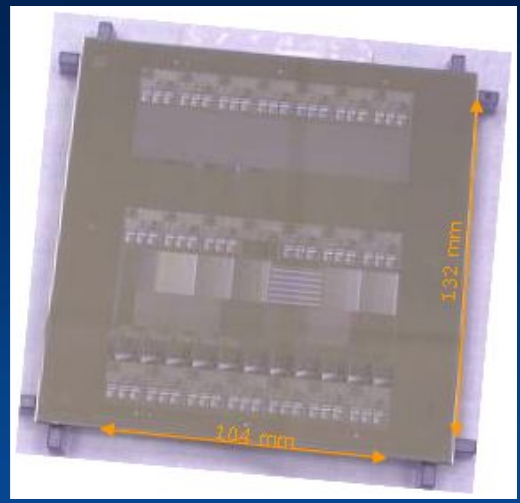
Lithography



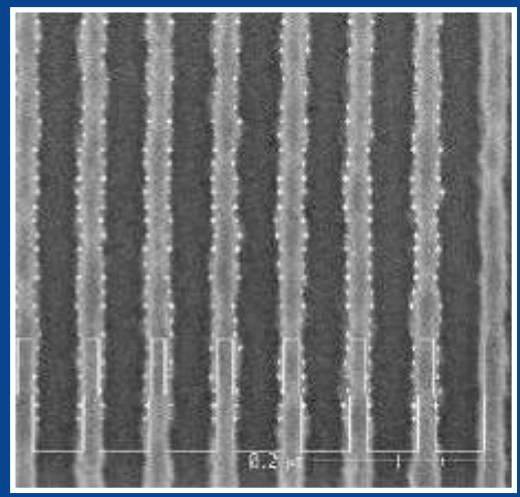
Extreme Ultraviolet is an option to extend lithography beyond the 32 nm generation

EUV Lithography

Operational EUV Research Tool

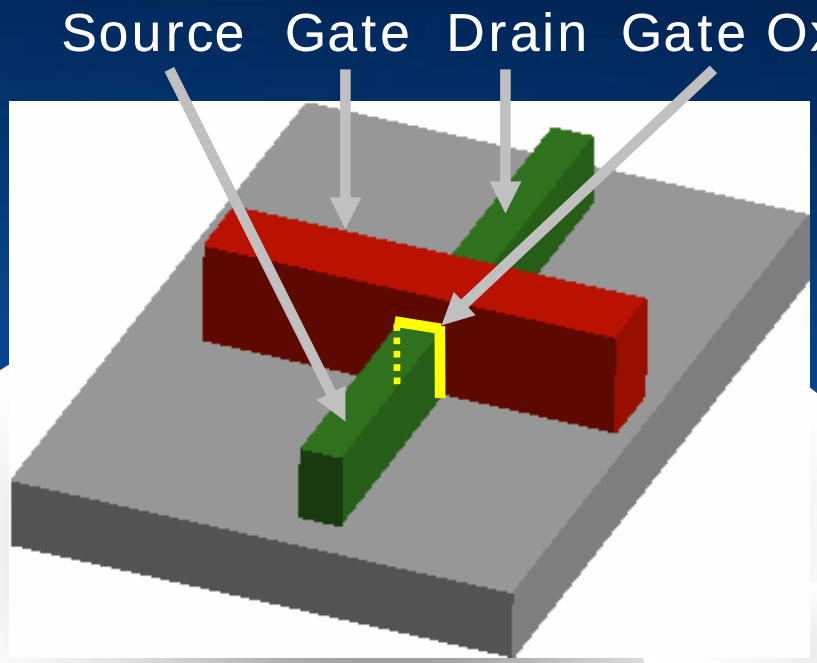


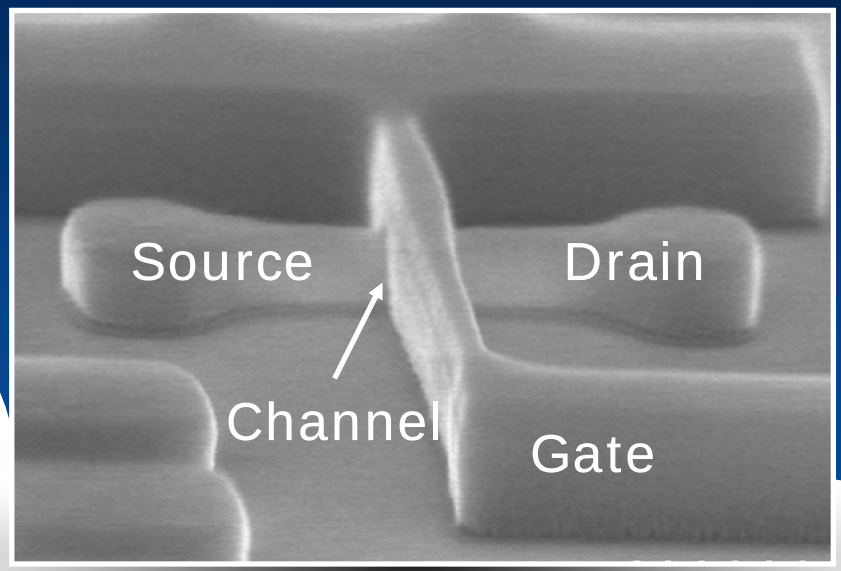
EUV Mask



26 nm line
78 nm pitch

Tri-Gate Transistors



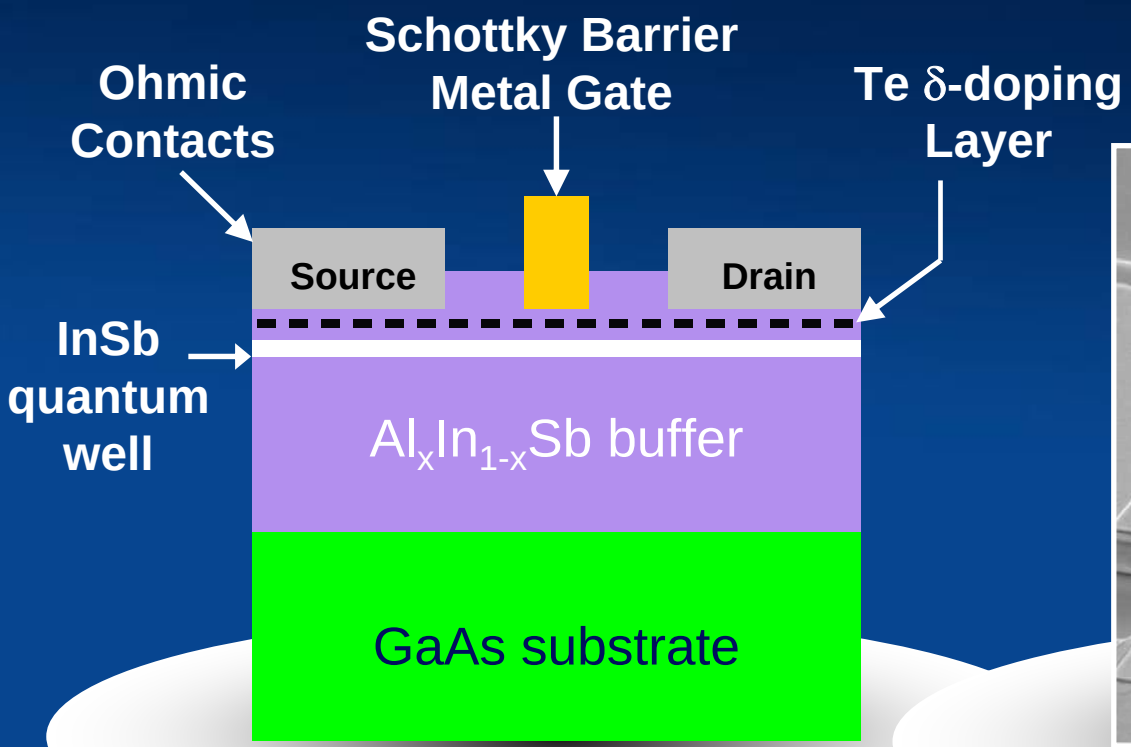


Transistor gate wraps around 3 sides of Si channel

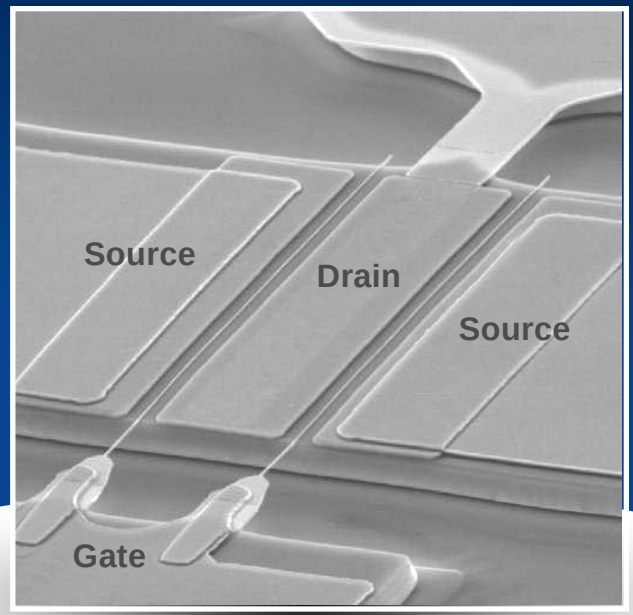
Transistor channel is fully depleted

Fully depleted operation reduces source-drain leakage

InSb Quantum Well Transistors



InSb Transistor



InSb Transistor

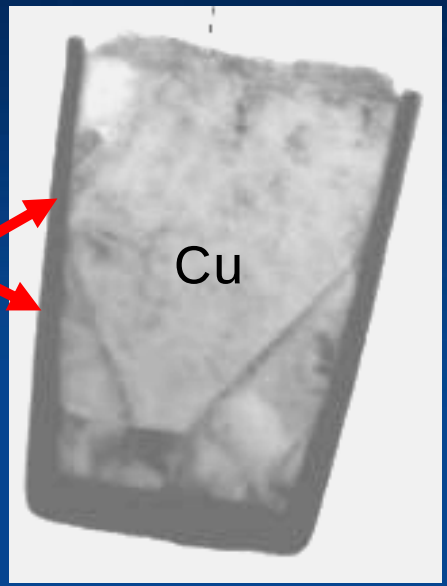
Electron mobility is ~50x higher in InSb than in Si

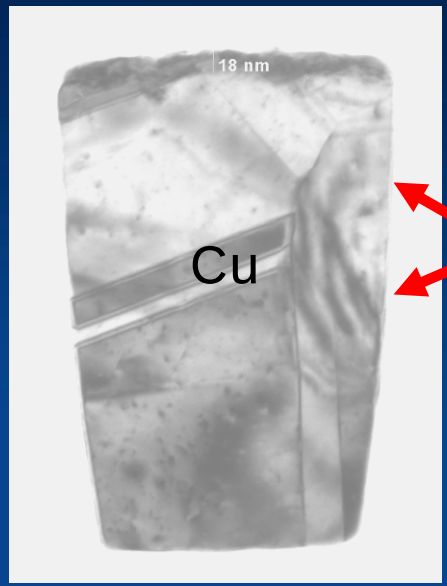
Increased mobility can lead to higher performance and less energy consumption

Interconnects

Physical Vapor Deposition (PVD)

Barrier





Atomic Layer Deposition (ALD)

Barrier

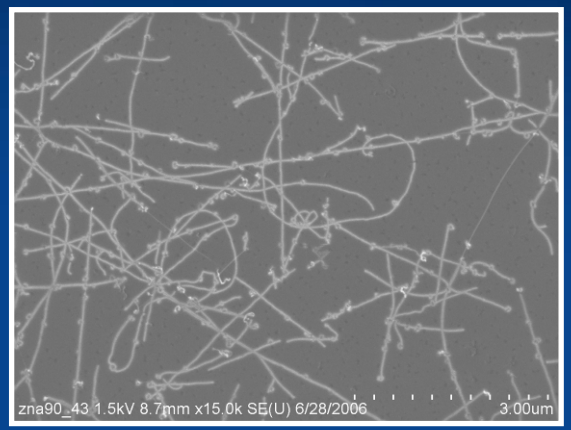
Focus Areas

Barrier thickness scaling

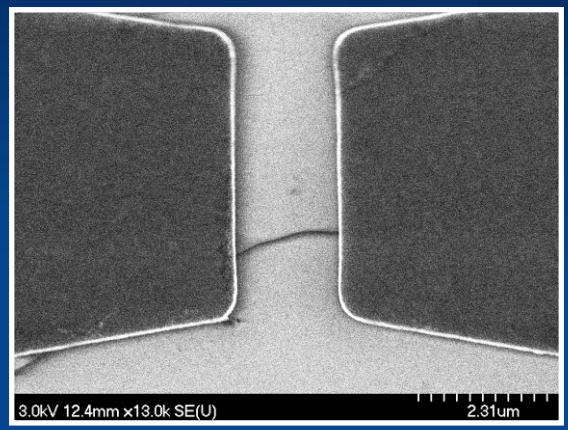
Interaction with Cu grain growth

Interaction with dielectric layer

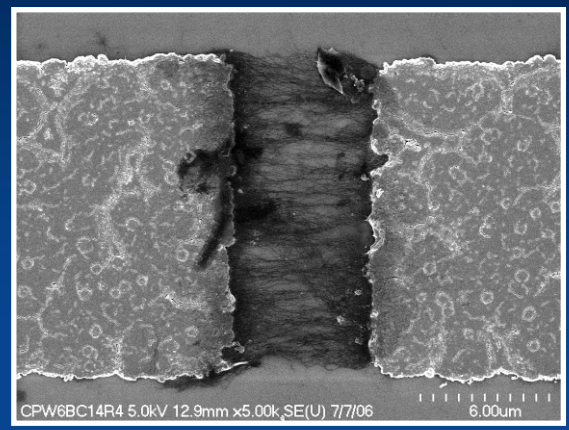
Carbon Nanotube Interconnects



CNT as grown



Aligned single CNT

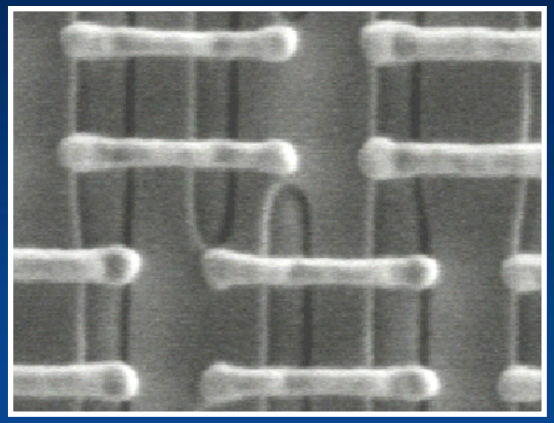


Aligned CNT bundle
(few thousand CNT)

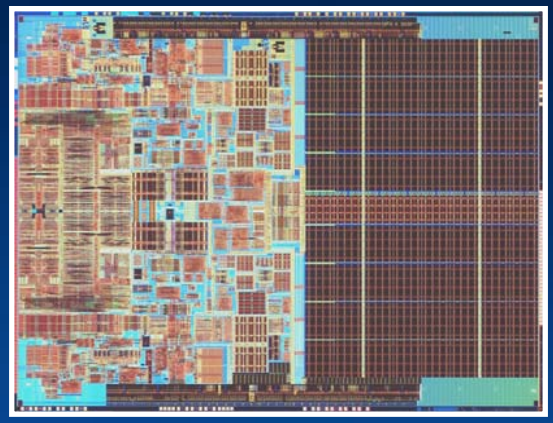
Outline

- Intel's Silicon R&D Pipeline
- Technologies in Manufacturing
- 45 nm High-k + Metal Gate Transistors
- Future Technology Options
- Summary

Intel Only: In-House Co-Optimization

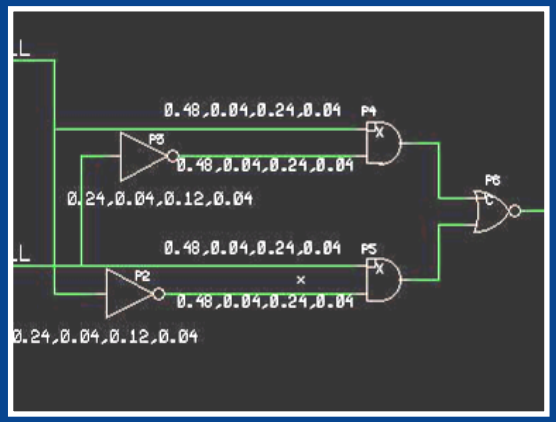


Process

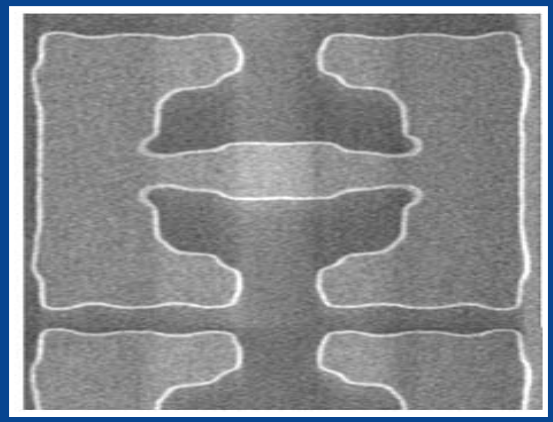


Products

Leading-edge Capacity



Design Tools



Masks

Packaging

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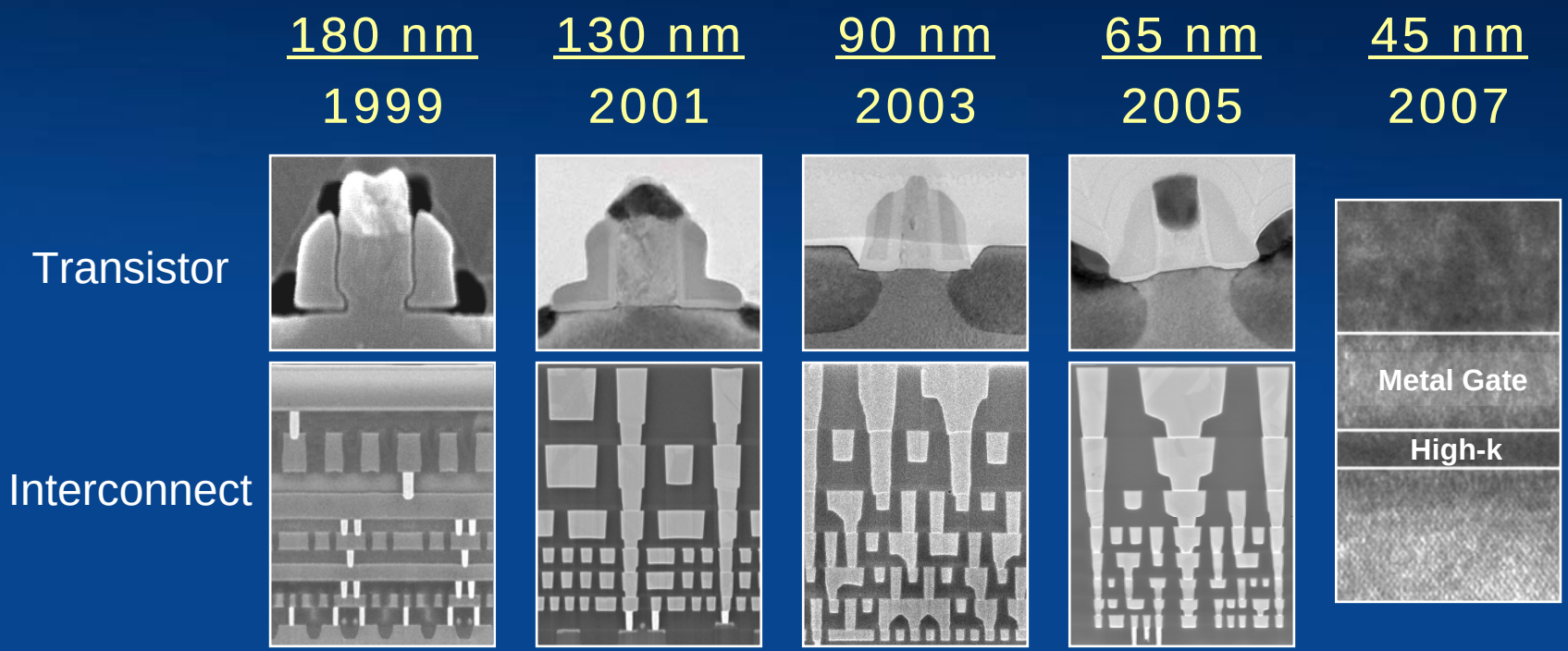
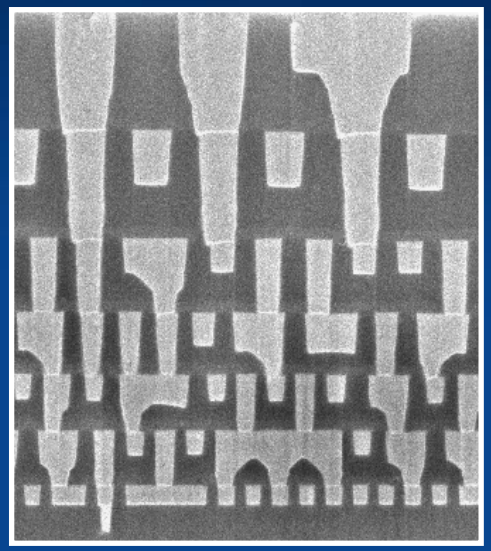
Intel Only: On-Time 2 Year Cycle

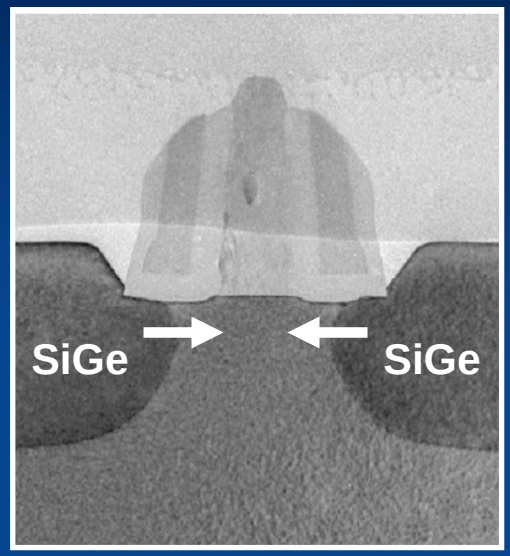


Reliable technology introduction dates

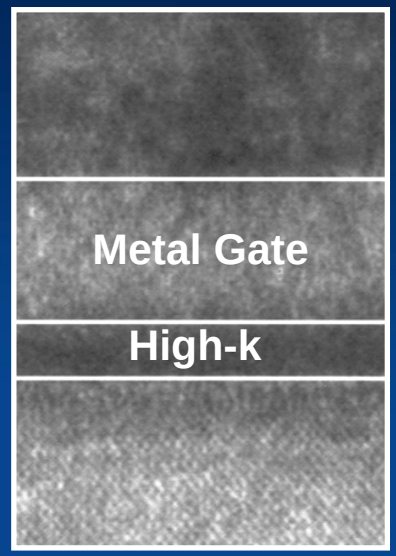
The New Era of Scaling



Copper + Low-k



Strained Silicon



High-k + Metal Gate

Modern CMOS scaling is as much about material innovation as dimensional scaling

Innovation-Enabled Technology Pipeline

90 nm
2003

65 nm
2005

45 nm
2007

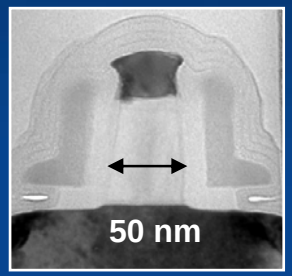
32 nm
2009

2011+

Manufacturing

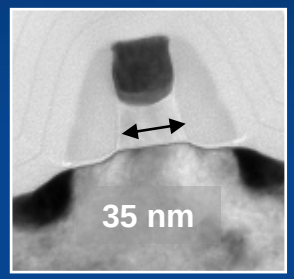
Development

Research



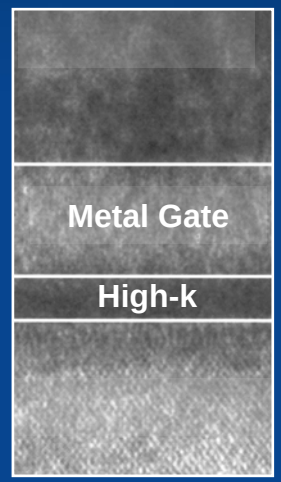
SiGe S/D

Strained Silicon

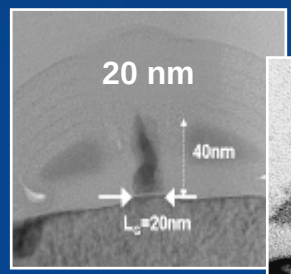


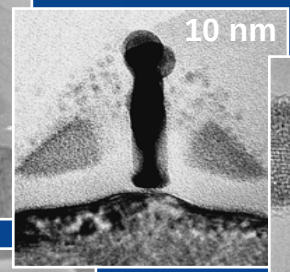
SiGe S/D

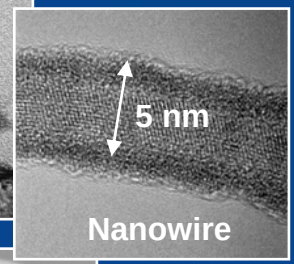
2nd generation Strained Silicon

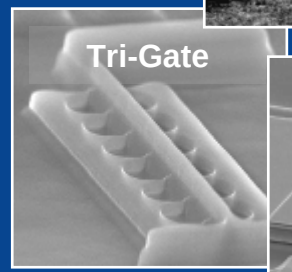


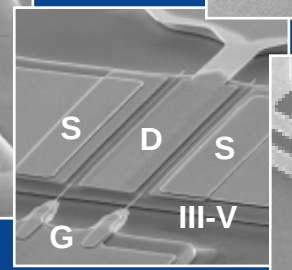
High-k Metal gate

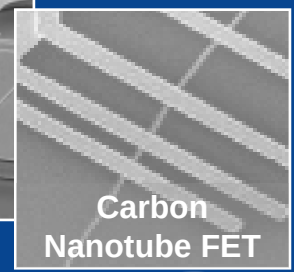












Future options subject to change

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Key Messages

- Intel's R&D pipeline will sustain Moore's Law for the foreseeable future
- Intel technologies are proliferated into a world-wide network of factories and Intel has a large presence in China
- 45 nm high-k + metal gate is the most significant innovation in transistor technology in 40 years
- Intel continues its unwavering commitment to support R&D for future technologies and to deliver the benefits of Moore's Law to our customers


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